REMARKS

Status of Claims:

While the Examiner has indicated in the outstanding Office Action that claims 1-31 are pending, applicant points out that the previously filed amendment (filed 10/08/04) added claim 32. Thus, claims 1-32 are present for examination.

Attorney Docket Number:

Applicant points out that in the previously filed amendment (filed 10/08/04), applicant requested that the attorney docket number be amended to be 024299-0352. Applicant notes that the Examiner has not amended the attorney docket number. Thus, applicant again requests that the attorney docket number be amended to be 024299-0352.

Claim Rejection under 35 U.S.C. 112

Claims 1-10 and 25-31 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

With respect to claims 1-10 and 25-31, the rejection is respectfully traversed.

The Examiner states that, "[t]he added material which is not supported by the original disclosure is as follows: Applicant replaced incrementing with modifying." (Emphasis Added). The Examiner also states that, "Increments address value is different than modifies address data." (Emphasis Added).

Applicant believes that "modifying" is supported by the specification for at least the following two reasons.

First, if address data is incremented, then it is modified. The Examiner recognizes that modifying address means the address "can be changeable or adjustable." Even under the Examiner's definition of "modifying", the act of incrementing is a form of modifying, because

address data that is incremented is changed and adjusted to be a next higher value. Thus, "modifying" is supported in the specification by "incrementing".

Second, the specification does not limit integrated circuits (ICs) to only incrementing address data. For example, as described in the specification, logic circuitry may be employed to **decrement** a counter sum by one to enable storage of a zero address in response to receipt of a single pulse as address data, and then an output generator may increment the value stored in the register by **two** and produce a corresponding number of pulses. (Specification; page 5, lines 12-20). Such logic circuitry "modifies" the address data by first decrementing by one and then incrementing by two.

Thus, the recitation of "modifying" is supported in the original specification and, therefore, claims 1-10 and 25-31 are believed to be in compliance with the requirements of 35 U.S.C. 112, first paragraph.

Claim Rejection under 35 U.S.C. 102

Claims 11-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Andreas (Pub. No. US 2004/0093450).

With respect to claims 11-24, the rejection is respectfully traversed.

Independent claim 11 recites an electronic device comprising:

> "a controller;
>
> a plurality of integrated circuits (ICs) addressable by the controller; and
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> a shared bus joining the controller and the plurality of integrated circuits;
>
> wherein the controller is programmed to produce a series of addresses **on the shared bus** and to produce an enable signal on an output in conjunction with a first address of the series of addresses,

wherein each of the ICs comprises an input for receiving an enable signal and an output for providing an enable signal in conjunction with a change in address data on the shared bus, and **means for storing an address** present on the shared bus **as an address of the IC** in response to receiving an enable signal, and

wherein the input of a first IC communicates with the output of the controller and the inputs of succeeding ICs communicate with the outputs of preceding ICs in a daisy chain configuration." (Emphasis Added).

An electronic device including the above-quoted features has the advantage that a controller can produce a series of addresses on a shared bus line and each IC can store an address that is present on the shared bus line as an address of the IC upon receiving an enable signal through a daisy chain configuration. Also, each IC comprises an output for providing an enable signal in conjunction with a change in address data on the shared bus. Such a configuration allows for IC addresses to be distributed over a shared bus while ensuring that each IC receives the correct address from the shared bus. (Specification; page 2, line 26 to page 3, line 4; page 6, line 7 to page 8, line 7).

In rejecting claim 11, the Examiner cited the following portions of Andreas: (a) [fig. 1, 110], [0025]; (b) [0021-0022], [fig. 2]; (c) [0021-0022]; (d) [0023-0026]; (e) [0026-0031]; and (f) [0025-0027]. However, those cited portions of Andreas actually refer to two separate embodiments of the invention in Andreas, which have mutually different structures and mutually different methods of operation. In particular, figure 1 and paragraphs [0021-0025] of Andreas relate to one embodiment, while figure 2 and paragraphs [0026-0031] of Andreas relate to a different embodiment. Each of the embodiments will now be described in turn, and then patentable differences of an electronic device including the above-quoted distinctions with respect to the system of Andreas will be discussed.

In the embodiment shown in figure 1 and described in paragraphs [0021-0025] of Andreas, a bus master 110 is coupled to a plurality of serial devices 120-150 sharing a common serial communications bus 160. (Andreas; paragraph [0021]). Each serial device has a chip select input (CS) that is asserted to indicate that the chip should respond to information being

broadcast on the serial communications bus. (Andreas; paragraph [0024]). In order to support unique identification of the serial devices, the bus master 110 must be capable of providing individual chip selects, one for each serial device. (Andreas; FIG. 1, references 172, 174, 176, 178; paragraph [0024]). Thus, the serial devices 120-150 are **not** assigned addresses, because if the bus master 110 wants a serial device to perform an operation, then the bus master just asserts the chip select signal for that serial device. (Andreas; paragraph [0024]). As Andreas recognizes, the disadvantage to such a system is that the bus master 110 must include a separate chip select signal for each serial device. (Andreas; paragraph [0004], [0024]).

Andreas does mention that "[t]he serial communication bus 160 carries commands, **addresses**, and data between the bus master and the serial devices." (Andreas; paragraph [0021]) (Emphasis Added). However, the addresses referred to by Andreas are **not** addresses of the serial devices 120-150. This is an important point that is not addressed in the Office Action: the addresses referred to by Andreas are **not** addresses that are assigned to the serial devices 120-150. Indeed, the serial devices 120-150 are **never assigned addresses** in the system of Andreas. The serial devices 120-150 in the embodiment of FIG. 1 of Andreas are enabled by a chip select signal that is unique for each serial device 120-150, so there is no need to further specify addresses to enable the serial devices, because they can already be enabled using chip select signals. (Andreas; paragraph [0024]).

Instead, the addresses referred to in Andreas are used for specifying a command that should be performed by a serial device that has already been enabled by a chip select signal. (Andreas; paragraphs [0023], [0025]). As stated in Andreas, "the command word includes a plurality of **address bits A0-A6**, and a R/W bit to indicate whether a read or a write operation is to be performed on the indicated address." (Andreas; paragraph [0025]) (Emphasis Added). Thus, the address bits A0-A6 in the system of Andreas do **not** specify an address of a serial device 120-150, but specify an address for a read or a write operation that is performed at an indicated address by a serial device that is already enabled by a **chip select signal**. (Andreas; paragraph [0025]).

Andreas does not specifically disclose what the indicated address refers to, but since the indicated address is used for a read or a write operation, Andreas suggests that the indicated address specifies a location in a memory. (Andreas; paragraph [0025]). It would not make sense in the system of Andreas for the address to represent an address of the serial device that receives the address, because the serial device would already have been selected based on the chip select signal to perform the operation. If the operation was to be performed on the serial device's own address, there would be no reason to send **additional** bits for the address, because the serial device would already have been selected to perform the operation on its own address when enabled by the chip select signal.

More concretely, the serial devices 120-150 perform an operation when they are enabled by a corresponding chip select signal. (Andreas; paragraph [0023]). The serial devices 120-150 do **not** check the address bits A0-A6 of the command words to determine if they are to perform an operation, because they already know whether or not they are to perform an operation based on the chip select signal. The address bits A0-A6 do **not** specify an address of a serial device, but specify an address for a read or a write operation that is to be performed by a serial device that is enabled by a separate chip select signal. (Andreas; paragraph [0025]). In contrast, the present claim recites a plurality of addressable ICs and that each of the ICs comprises means for storing an address present on a shared bus as an address of the IC.

In the embodiment shown in FIG. 2 of Andreas, a bus master 210 is coupled to a plurality of serial devices 220-250 sharing a common serial bus 260. In contrast to the embodiment of FIG. 1, the embodiment of FIG. 2 has a single chip select signal that is shared among multiple serial devices 220-250. (Andreas; paragraph [0029]). Thus, Andreas recognizes that, "**other mechanisms** must be used to **differentiate** between chips in the same group." (Andreas; paragraph [0029]) (Emphasis Added). The embodiment shown in FIG. 2 of Andreas does **not** assign addresses to the serial devices 220-250 to differentiate the serial devices. Instead, the serial devices 220-250 in the embodiment of FIG. 2 of Andreas are enabled or disabled based on a chip select signal and a mask value. (Andreas; paragraph [0030]). The mask value is **not** an

address that is assigned to a serial device. Rather, each bit in the mask value is associated with a corresponding serial device, so that if a bit is '1' in a particular mask value the corresponding serial device is enabled, but if the bit is '0', then the corresponding serial device is disabled. (Andreas; paragraph [0040]). In order to enable and disable the serial devices, the mask value must be **clocked through** all of the devices before each operation. (Andreas; paragraph [0036]).

In view of the above described structures and operations of the embodiments in Andreas, it is evident that Andreas neither discloses nor suggests an electronic device including the above-quoted features. An electronic device including the above-quoted features allows for assigning addresses to ICs and, thus, allows for initializing IC addresses. (Applicant's Specification; page 1, lines 6-7; page 7, lines 3-4). Since the serial device slaves 120-150 and 220-250 in the system of Andreas do not require addresses for operation, Andreas neither discloses nor suggests a system in which serial device slaves are assigned addresses.

More specifically, Andreas neither discloses nor suggests the claimed feature, "wherein each of the ICs comprises an input for receiving an enable signal and an output for **providing an enable signal** in conjunction with a change in address data on the shared bus, and means for storing an address present on the shared bus **as an address of the IC** in response to receiving an enable signal". (Emphasis Added). The Examiner points to Andreas, paragraphs [0026-0031], as disclosing such a feature. However, the Examiner has not indicated what data bits in the system of Andreas are stored by a serial device slave as an address of the serial device slave. Indeed, Andreas does not disclose or suggest storing address data as an address of a serial device.

As discussed above, the address bits A0-A6 in the system of Andreas are not stored by a serial device slave as an address of the serial device slave, but are used by a serial device slave to perform a read or a write operation at the address indicated by the bits A0-A6. (Andreas; paragraph [0025]). Furthermore, the mask value bits S0-S7 in the system of Andreas are not stored by a serial device slave as an address of the serial device slave, but each serial device slave only checks a certain bit of the mask value to determine whether or not it is enabled for a particular operation. (Andreas; paragraphs [0036], [0041]). In addition, the mask value is not

even sent on a shared bus, but is sent as part of an SDI signal, and Andreas states that, "[t]he SDI signal is not part of the shared communication bus 260", and that, "[e]ach serial device receives its SDI signal from a preceding device rather than from the serial communication bus 260." (Andreas; paragraph [0026]) (Emphasis Added).

In an electronic device including the above-quoted features, a plurality of ICs are addressable by a controller, and each IC comprises means for storing an address present on a shared bus as an address of the IC. Thus, such an electronic device allows for initializing addresses of the ICs on the shared bus. In contrast the address bits A0-A6 in the system of Andreas are **not** an address of a serial device on a communications bus.

Therefore, independent claim 11 is neither disclosed nor suggested by the cited prior art and, hence, is believed to be allowable.

If the Examiner persists in the rejection of claim 11, applicant requests that the Examiner specifically explain what the Examiner considers to be the address that is present on a shared bus and that is stored by a serial device slave as an address of the serial device slave. Also, applicant requests that the Examiner specifically indicate where Andreas discloses that a serial device slave has an output for providing an enable signal in conjunction with a change in address data on a shared bus.

Because they depend from claim 11, dependent claims 12-19 and 32 are believed to be allowable for at least the same reasons that claim 11 is believed to be allowable.

Independent claim 20 recites an electronic device with features similar to features of an electronic device of independent claim 11. Therefore, claim 20 is believed to be allowable for at least the same reasons that claim 11 is believed to be allowable.

Independent claim 21 recites a method for initializing addresses of a plurality of integrated circuits with features similar to features of an electronic device of independent claim

11. Therefore, claim 21 is believed to be allowable for at least the same reasons that claim 11 is believed to be allowable.

Because they depend from claim 21, dependent claims 22-24 are believed to be allowable for at least the same reasons that claim 21 is believed to be allowable.

Claim Rejections under 35 U.S.C. 103

Claims 1-10 and 25-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andreas in view of Floyd et al. (U.S. Patent Number 6,529,979) (hereinafter Floyd).

With respect to claims 1-10 and 25-31, the rejection is respectfully traversed.

Independent claim 1 recites an electronic device comprising:

> "a controller programmed to produce first address data on an output thereof;
>
> a plurality of integrated circuits (ICs) addressable by the controller; and
>
> a shared bus joining the controller and the plurality of ICs;
>
> wherein each of the ICs comprises an input for receiving address data **representing an address of the IC on the shared bus**, and an output for providing **modified** address data different from the received address data, and
>
> wherein the input of a first IC communicates with the output of the controller and the inputs of succeeding ICs communicate with the outputs of preceding ICs in a daisy chain configuration." (Emphasis Added).

An electronic device including the above-quoted features has the advantage that a controller produces a first address for a first IC, and each IC has an input for receiving address data **representing an address of the IC** and an output for providing **modified** address data to a succeeding IC in a daisy chain configuration. Thus, each IC in the daisy chain is provided with an address. Each IC may then use its address to distinguish whether or not a communication on

the shared bus is intended for that IC. (Specification; page 1, lines 23-24; page 2, lines 20-26; page 5, lines 1-11).

Neither Andreas nor Floyd, alone or in combination, disclose or suggest an electronic device including the above-quoted features. In response to applicant's remarks filed on 10/08/04, the Examiner stated:

> "In response to applicant's argument that in Andreas the slave devices are never assigned an address. Examiner respectfully disagrees. As Andreas notes at [0021-0026] discloses the communication between master 110 and devices 120-150 via sharing bus 160. The sharing bus 160 carries commands, addresses and data between the master and devices. Each command associated with specific address for specific device. In order to select a specific device the unique identification of each device must be provided by master. [0021-0026]." (Emphasis Added).

The Examiner appears to be equating the addresses carried on the communications bus 160 with the unique identification of each device that is provided by the bus master 110. However, the addresses carried on the communications bus 160 are not addresses of the serial devices 120-150 on the communications bus 160. The unique identification of the serial devices 120-150 is not provided by having each of the serial devices 120-150 receive address data representing an address of the serial device on the communication bus 160. Instead, the unique identification in the system of Andreas is provided by using chip select signals. (Andreas; paragraphs [0023-0024]).

As stated in Andreas, "[e]ach serial device has a chip select input (CS) that is asserted to indicate that the chip should respond to information being broadcast on the serial communications bus." (Andreas; paragraph [0024]). Also, as stated in Andreas, "[i]n order to support unique identification of a plurality of serial devices using the chip select signals, bus master 110 must be capable of providing individual chip selects, one for each serial device." (Andreas; paragraph [0024]; FIG. 1, references 172, 174, 176, 178) (Emphasis Added). Thus, the unique identification of the serial devices 120-150 is provided by the individual chip select signals 172-178 to each of the serial devices, and not by addresses of the serial devices 120-150

on the communications bus 160. The addresses carried on the communications bus 160 are not addresses representing addresses of serial devices 120-150, but are addresses for read or write operations to be performed by a serial device at an indicated address. (Andreas; paragraph [0025]).

Moreover, the Examiner recognizes that Andreas does not disclose providing modified address data different from the received address data. The Examiner points to Floyd as disclosing, "the address packet modified in a variety of different manners to provide an indication of a positive acknowledgement, such as modifying other bits, adding other bits, or otherwise modifying the format of the address packet on the return path to the originator of the address packet." (Emphasis Added) The Examiner then states that, "[i]t would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Floyd's teaching into Andreas's system so as to have the advantages to improve communication system and protocol for dedicated configuration to minimizes the amount of circuitry and wire congestion." (Emphasis Added).

However, with an electronic device including the above-quoted features, each of the ICs comprises an input for receiving address data representing an address of the IC on the shared bus, and an output for providing modified address data different from the received address data. Also, with an electronic device including the above-quoted features, the output of a first IC communicates with the output of the controller and the inputs of succeeding ICs communicate with the outputs of preceding ICs. Thus, in an electronic device including the above-quoted features, when an IC provides modified address data different from the received address data at an output, the modified address data represents an address of the succeeding IC on the shared bus that is received by the input of the succeeding IC.

In contrast, in the apparatus of Floyd, an address is modified to provide a positive acknowledgement, and not to provide an address of a succeeding satellite on a serial bus. (Floyd; abstract). For example, Floyd teaches that an incoming address may be re-sent by a satellite unchanged, except for gating off a stop bit, which is used for positive acknowledgement. (Floyd;

abstract; column 7, lines 26-58). Thus, Floyd does not disclose or suggest to have satellites receive addresses representing addresses of the satellites on a shared bus and to provide modified addresses that represent addresses of succeeding satellites on the shared bus.

Furthermore, even if Floyd's teachings were incorporated into Andreas's system, the addresses that would be modified would not even be addresses of serial devices 120-150 on the communications bus 160 because, as explained above, the addresses referred to in Andreas are not addresses of the serial devices 120-150. (Andreas; paragraph [0025]).

Therefore, independent claim 1 is neither disclosed nor suggested by the cited prior art and, hence, is believed to be allowable.

Because they depend from claim 1, dependent claims 2-7 and 25-28 are believed to be allowable for at least the same reasons claim 1 is believed to be allowable.

Independent claim 8 recites an electronic device comprising:

> "means for generating first address data at an output of a controller;
>
> means for receiving the first address data at an input of a first IC;
>
> means for storing the first address data in the first IC as an address of the first IC;
>
> means for modifying the first address data in the first IC to produce first modified address data different from the first address data; and
>
> means for providing the first modified address data to a second IC through an output of the first IC."

Neither Andreas nor Floyd, alone or in combination, disclose or suggest an electronic device including the above-quoted features. The Examiner points to Andreas, paragraphs [0021-0023] as disclosing, "Means for storing the first address data in the first IC as an address of the first IC". (Emphasis Added). However, applicant can find no mention in the cited portions of Andreas of a means for storing an address as an address of a serial device. (Andreas; paragraphs

[0021-0023]). Indeed, as discussed above with respect to claim 1, the serial devices in the system of Andreas are never assigned addresses.

Therefore, independent claim 8 is neither disclosed nor suggested by the cited prior art and, hence, is believed to be allowable.

Because it depends from claim 8, dependent claim 29 is believed to be allowable for at least the same reasons that claim 8 is believed to be allowable.

Independent claim 9 recites a method for initializing addresses of a plurality of integrated circuits with features similar to features of an electronic device of independent claim 8. Therefore, claim 9 is believed to be allowable for at least the same reasons that claim 8 is believed to be allowable.

Because they depend from claim 9, claims 10 and 30-31 are believed to be allowable for at least the same reasons that claim 9 is believed to be allowable.

Conclusion:

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 50-0872. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 50-0872. If any extensions of time are needed for timely acceptance of papers

submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 50-0872.

Respectfully submitted,

Date April 29, 2005

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